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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

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10076458	02/19/2002	324	501	2858	TURESIWSP

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**CONTINUING DATA VERIFIED: *NO*

** FOREIGN APPLICATIONS VERIFIED: *ST*
JAPAN 2001-42356 02/19/2001
JAPAN 2001-111132 04/10/2001
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PG-PUB	DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>	ATTORNEY DOCKET NO
Foreign priority claimed <input checked="" type="checkbox"/> yes <input type="checkbox"/> no			0052/064001
35 USC 119 conditions met <input checked="" type="checkbox"/> yes <input type="checkbox"/> no			
Verified and Acknowledged Examiners's initials <i>ST</i>			

TITLE : Circuit board testing apparatus and method for testing a circuit board
U.S. DEPT. OF COMMERCE, PAT. & TM. PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Assistant Examiner	Total Claims: Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Primary Examiner	Sheets Drawn: Figs. Drawn: Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner
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